CLAIMS

1 A circuit comprising:

a pad circuit configured to transfer a data signal in response to a pad control signal;

a core logic configured to (i) exchange said data signal with said pad circuit and (ii) present a control signal;

a cell configured to (i) transfer said data signal between said pad circuit and said core logic and (ii) swap said data signal and a test signal; and

a test circuit configured to (i) exchange said test data signal with said cell, (ii) store a test control signal, and (iii) multiplex said test control signal and said control signal to present said pad control signal.

2. The circuit according to claim 1, wherein (i) said test circuit exchanges said test data signal with said cell by presenting said test data signal to said cell, (ii) said cell swaps said data signal and said test data signal by overwriting said data signal with said test data signal, and (iii) said cell exchanges said data signal with said pad circuit by said pad circuit receiving said data signal from said cell.

3. The circuit according to claim 2, wherein said test circuit is further configured to clock said test data signal to cause said data signal received by said pad circuit to change states.

4. The circuit according to claim 1, wherein (i) said cell exchanges said data signal between said pad circuit by pad circuit presenting said data signal to said cell, (ii) said cell swaps said data signal and said test data signal by overwriting said test data signal with said data signal, and (iii) said test circuit exchanges said test data signal with said cell by receiving said test data signal from said cell.

5. The circuit according to claim 4, wherein said test circuit is further configured to clock said test data signal to receive a sequence of samples for said data signal as received by said cell.

6. The circuit according to claim 1, wherein said test circuit comprises:

a multiplexer configured to multiplex said control signal and said test control signal to present said pad control signal; and

a controller configured to (i) store said test control signal, (ii) present said test control signal to said multiplexer, and (iii) exchange said test data signal with said cell.

7. The circuit according to claim 6, wherein said controller comprises:

an input configured to receive said test control signal; and

a user data register configured to (i) store said test control signal from said input and (ii) present said test control signal to said multiplexer.

8. The circuit according to claim 7, wherein (i) said test circuit exchanges said test data signal with said cell by presenting said test data signal to said cell, (ii) said cell swaps said data signal and said test data signal by overwriting said data

signal with said test data signal, (iii) said cell exchanges said data signal with said pad circuit by said pad circuit receiving said data signal from said cell, and (iv) said test circuit is further configured to clock said test data signal to cause said data signal received by said pad circuit to change states.

9. A method of testing a pad circuit that transfers a data signal in response to a pad control signal, the method comprising the steps of:

(A) generating a test control signal;

(B) multiplexing said test control signal and a control signal presented by a core logic in response to step (A);

(C) presenting said test control signal as said pad control signal to said pad circuit in response to step (B); and

(D) swapping said data signal of said pad circuit and a test data signal of a cell in response to step (C).

10. The method according to claim 9, wherein step (D) comprises the sub-steps of:

transferring said test data signal to said cell in response to step (C);

overwriting said data signal with said test data signal in response to said transferring; and

presenting said data signal to said pad circuit in response to said overwriting.

11. The method according to claim 10, further comprising the steps of:

clocking the test data signal in response to presenting said data signal to said pad circuit;

second overwriting said data signal with said test data signal in response to clocking; and

second presenting said data signal to said pad circuit in response to said second overwriting.

12. The method according to claim 11, further comprising the step of measuring a transition response of said pad circuit as said data signal changes from said presenting to said second presenting.

13. The method according to claim 1, wherein step (D) comprises the sub-steps of:

receiving said data signal at said cell in response to step (C);

overwriting said test data signal with said data signal in response to said receiving said data signal; and

transferring said test data signal from said cell in response to said overwriting.

14. The method according to claim 13, further comprising the steps of:

second receiving said data signal in response to transferring said test data signal;

second overwriting said test data signal with said data signal in response to said second receiving; and

second transferring said test data signal from said cell in response to said second overwriting.

15. The method according to claim 14, further comprising the step of measuring a transition response of said pad circuit as

said test data signal changes from said transferring from said cell to said second transferring from said cell.

16. A circuit comprising:

first means for transferring a data signal in response to a first control signal;

means for exchanging said data signal with said first means for transferring;

means for presenting a second control signal;

second means for transferring said data signal between said first means for transferring and said means for exchanging;

means for swapping said data signal and a test signal;

means for exchanging said test data signal with said second means for transferring;

means for storing a third control signal; and

means for multiplexing said third control signal and said second control signal to present said first control signal.